REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Claims 1-28 are pending.

Applicants note with appreciation the Examiner's indications that claims 20-28 are allowed.

Applicants further note with appreciation the Examiner's indication that claims 2-5, 8-10 and 12-18 would be allowable if placed in independent form. As discussed in detail below, Applicants believe that these claims depend from allowable claims, and for this reason, these claims have not been rewritten in independent form at this time.

The Examiner objects to claims 2-5 for minor informalities with respect to claim 2. Claim 2 has been amended in order to eliminate the informalities noted by the Examiner. These amendments are strictly clarifying, and are not narrowing.

Claims 1, 6, 7, 11 and 19 stand rejected under 35 U.S.C. §102(b) as being anticipated by Shin (U.S. Patent No. 6,342,801). Applicants respectfully traverse this art grounds of rejection.

In the art grounds of rejection, the Examiner relies upon the disclosure with respect to Figs. 1 and 2 of Shin. This disclosure relates to the operation control of DLL circuits discussed in the Background of the Invention section for the subject application. As discussed in detail in the Background of the Invention section of the subject application, these prior art DLL circuits are controlled such that they are in a powered down mode during a refresh operation of an SDRAM or DRAM. Similarly, Shin states in column 1, line 65 - column 2, line 4:

> The power mode controller 300 receives the operation code signal op_code and the control signal Cntrl from the packet controller 200 to generate the self-refresh enable signal Self_Refresh_en to the memory core 100 and the nap mode signals Nap and the power down mode signals PDN to the delay locked loop circuit 400.

As demonstrated above, prior art delayed lock loop circuits as in Figs. 1-2 of Shin are not supplied with power during a refresh operation. By contrast, the embodiments of the present invention are disclosed as supplying power to the DLL circuit during a refresh operation or not supplying power to a DLL circuit during a refresh operation based on a selection signal. Therefore, as recited in claim 1, a control signal generator selectively supplies power to the DLL circuit during a refresh mode. Since Shin always cuts power to the DLL circuit during a refresh mode, Shin cannot disclose or suggest selectively supplying power to the DLL circuit during a refresh mode.

Therefore, claim 1 is not anticipated or rendered obvious to one skilled in the art by Shin. Claims 6, 7 and 11, dependent upon claim 1, are patentable for the reasons stated above with respect to claim 1 as well as on their own merits. Claim 19 includes similar limitations to those discussed above with respect to claim 1, and is therefore patentable at least for the reasons stated above with respect to claim 1.

Applicants respectfully request that the Examiner withdraw this art grounds of rejection.

CONCLUSION

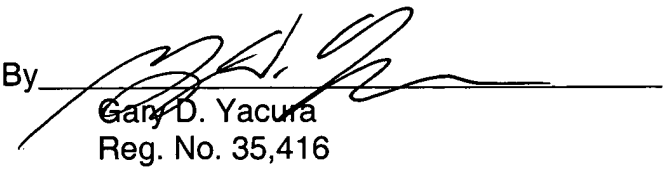
In view of above remarks, reconsideration of the outstanding rejection and allowance of the pending claims is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at number listed below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, PLC

By 

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